Serial No.: 10/770,711
Group Art Unit: 2825

REMARKS

Claim Objections

Claims 1–20 were objected to because of various possible informalities. Claims 1–20 have therefore been amended as suggested by the Examiner.

It is especially and particularly pointed out that the above amendments to claims 1–20 are in response only to the Examiner's concerns about possible informalities therein, and are directed strictly thereto. The amendments are in no way intended to, or in fact do, change the scope of these claims. (*In re* Festo.)

Claim Rejections - 35 USC §102

Claims 1-20 are rejected under 35 U.S.C. §102(b) as being anticipated by Kulkarni et al. (U.S. Patent No. 5,991,699, hereinafter "Kulkarni").

Kulkarni provides for detecting groups of defects in semiconductor feature space. Techniques for improving manufacturing process control are based on inspection of manufactured items at intermediate process steps, based on clustering and binning of defect data, and specifically relating to semiconductor manufacturing process control. Examples relate specifically to semiconductor wafers, but may be generalized to any manufacturing process.

Summary of Applicant's Arguments

Kulkarni is directed to identifying and correcting wafer process steps to minimize the recurrence of similar defects in later produced wafers in later production runs. Kulkarni does not address the question of what to do with existing intermediate wafers that already have defects.

The present invention discloses and claims methods and systems for making intelligent decisions concerning the disposition of partially completed wafers that have already acquired defects. As pointed out in the present application, each finished semiconductor wafer has hundreds to tens of thousands of integrated circuits ("ICs"), each

worth hundreds or thousands of dollars. The decision whether or not to finish processing a partially defective wafer lot is therefore a crucially important economic decision. For example, many ICs (e.g., memory chips) with minor defects can still be perfectly serviceable because they contain redundancies allowing defective elements to be mapped out.

But it is not always readily determinable how serious an intermediate defect is, and whether the defect will be "fatal", or will cause only minor consequences.

The present invention, as disclosed and claimed, enables such "proceed or stop" decisions to be made by disclosing the future effects upon later layers of current defects.

Kulkarni has no such disclosure. Kulkarni does not address or facilitate subsequent disposition ("proceed or stop") decisions.

Kulkarni accordingly fails to anticipate the present invention under 35 USC §102(b). The rejection should therefore be withdrawn, the claims should be allowed, and the application should be passed to issuance.

Detailed Response to the Rejection

Regarding claims 1 and 11, the Applicant respectfully traverses the rejection since the Applicant's claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Kulkarni of:

> "generating at least one layer model from the information and data to disclose the effects of the at least one defect upon at least one later layer of the semiconductor wafer; and
> utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot."

The Examiner states in the Final Office Action dated July 31, 2006:

> "(c) generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor layer (see col. 9, line 45 — col. 10, line 7; col. 22, ll. 26 - 37); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again Abstract; col. 3, line 60 – col. 4, line 10; col. 10, ll. 12 - 33)."

However, Kulkarni does not disclose disclosing the effects of the at least one defect upon at least one later layer of the semiconductor wafer and utilizing it to determine the subsequent disposition of the wafer production lot. Instead, in the sections cited by the Examiner (quoted and identified below), Kulkarni merely states:

> "A more consistent identification of defects on a semiconductor wafer...make it possible to make changes in various aspects of the manufacture of the semiconductor devices with which it is used, as well as suggesting changes to the inspection, defect review and manufacturing processes; and as to the classification of defects, the detection of defects that occur repeatedly, and the detection of the process steps that constitute the defect causal mechanisms.
>
> A variety of defect properties are typically measured...In this manner the data of the entire defect population is gradually identified... thus reducing unidentified data...to determinable specific causes and individual defects for later identification." (col. 9, line 45 – col. 10, line 7) [deletions and underlining for clarity]

> "Here spatial clustering on the entire set of defects on the wafer is performed...and the corrected defect count are stored..." (col. 22, ll. 26 - 37) [deletions for clarity]

> "Techniques for improving manufacturing process control...may be generalized to any manufacturing process." (Abstract) [deletions and underlining for clarity]

> "The present invention provides a system and method to identify defect groups that have a common causality...In so doing it is also more likely that the causation of the defect cluster could be determined thus enabling the identification of the corrective actions that are necessary to reduce or eliminate the occurrence of further defects from that identified causation...thus dramatically increasing the yield of a particular type of wafer that will result in reduced production costs and long term reliability of the individual components produced from the die on that wafer." (col. 3, line 60 – col. 4, line 10) [deletions and underlining for clarity]

> "In the present invention...clustering, characteristics such as physical spacing, defect size, defect shape, etc., that are typical of defects that are known to occur in a particular production step just completed for the type of material and wafer size being produced by known defect causal mechanisms in those situations are considered." (col. 10, ll. 12 - 33) [deletions for clarity]

Thus Kulkarni discloses only the correction of existing defect-producing mechanisms, and discloses nothing about determining the disposition of an existing partially completed,

defect-containing wafer lot. Kulkarni thus does not disclose disclosing the effects of the at least one defect upon at least one later layer of the semiconductor wafer and utilizing it to determine the subsequent disposition of the wafer production lot as claimed in claims 1 and 11.

Based on the above, it is respectfully submitted that independent claims 1 and 11, and the respective claims 2–5 and 12–15 depending therefrom, are allowable under 35 USC §102(b) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejection is therefore respectfully requested.

Pursuant to claims 2 and 3, these dependent claims each depend from independent claim 1 and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 2 and 3 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

The Applicant also respectfully traverses the rejection of claims 2 and 3 since the Applicant's claimed combination includes the limitation not disclosed in Kulkarni of:

> "disclosing the components that will be located above the at least one defect in the semiconductor wafers" (claim 2)
>
> and
>
> "treating the data concerning the at least one defect as a new layer of information"

The Examiner states in the Office Action:

> "Pursuant claims 2 and 3 see col. 2, ll. 53 – 62; col. 3, ll. 47 – 57; col. 22, ll. 27 - 37, which disclose the limitations pertaining to generating and

> utilizing a layer model to determine subsequent disposition of the wafer production lot (claim 3), and suggesting the locations of components above a defect in a wafer (claim 2)."

However, Kulkarni does not disclose disclosing the components that will be located above the at least one defect in the semiconductor wafers (claim 2) or treating the data concerning the at least one defect as a new layer of information (claim 3). Instead, in the sections cited by the Examiner (quoted and identified below), Kulkarni merely states:

> "Correlation studies of defect locations on a given wafer inspected at one step in the manufacturing process may be performed against the inspection results for the same wafer at a different process step, in order to determine the process step that is the source of particular defects or defect types. Identification of the processing step that is the source of a defect is a necessary condition for eliminating that source of the defects. Correlation studies of defects on one die may also be compared against other dies to identify repeating defects." (col. 2, ll. 53 – 62) [underlining for clarity]

> "It would prove very beneficial if group defects could be placed into certain meaningful cluster approximations of those groups...which would make defect data much more manageable. Then it would be even more beneficial if that more manageable cluster defect data could be processed automatically to identify corrective actions necessary to reduce the number of defect groups, and therefore total number of defects, that occur in later production runs. The present invention provide such a system" (col. 3, ll. 47 – 57) [deletions and underlining for clarity]

> "Here spatial clustering on the entire set of defects on the wafer is performed...and the corrected defect count are stored..." (col. 22, ll. 27 - 37) [deletions for clarity]

Thus, Kulkarni discloses searching for the source of particular defects and identifying the individual processing step that is the source of the defect. As stated in the first quote above (col. 2, ll. 53 – 62), the search for that one cause may span different process steps, but that is not the same as disclosing the components that will be located above the at least one defect in the semiconductor wafers (claim 2) or treating the data concerning the at least one defect as a new layer of information (claim 3).

Accordingly, Kulkarni makes no reference to nor discloses disclosing the components that will be located above the at least one defect in the semiconductor wafers (claim 2) or treating the data concerning the at least one defect as a new layer of information (claim 3), as

claimed. Allowance of claims 2 and 3 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Pursuant to claim 4, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and additionally claims non-obvious combinations thereof. Allowance of claim 4 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

The Applicant also respectfully traverses the rejection of claim 4 since the Applicant's claimed combination includes the limitation not disclosed in Kulkarni of:

> "determining whether the at least one defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers"

The Examiner states in the Office Action:

> "As for claim 4, see col. 9, line 45 – col. 10, line 64, which cites the likely cause and clustering of possible defects in a production wafer lot, as claimed."

However, Kulkarni makes no reference to nor discloses bridging, an open circuit, or blockage as claimed in claim 4. Allowance of claim 4 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Pursuant to claim 5, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and additionally claims non-obvious combinations thereof. Allowance of claim 5 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claims 6 and 16, the Applicant respectfully traverses the rejection since the Applicant's claimed combination, as exemplified in claim 6, includes the limitation not disclosed in Kulkarni of:

"generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process; and
utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot."

The Examiner states in the Final Office Action dated July 31, 2006:

> "(c) generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the process (see col. 9, line 45 – col. 10, line 7; col. 22, ll. 26 - 37); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again Abstract; col. 3, line 60 – col. 4, line 10; col. 10, ll. 12 - 33)."

However, these same cited sections from Kulkarni and these same issues have been discussed in detail above with respect to the rejection of claims 1 and 11, and those arguments are equally applicable to the rejection of claims 6 and 16, showing that Kulkarni does not disclose generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process, and utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, as claimed.

Likewise, the rejections of claims 7–10, 12–15, and 17–20 are respectively reflections of the corresponding rejections of claims 2–5, presenting and raising the same respective substantive issues and citing the same respective portions of Kulkarni. Accordingly, these same issues have been discussed in detail above with respect, respectively, to the rejections of claims 2–5. Those corresponding arguments above on behalf of the Applicant are therefore equally applicable to the rejections of claims 7–10, 12–15, and 17–20, as discussed and explained above.

It is therefore respectfully submitted that independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are allowable under 35 USC §102(b). Allowance of claims 1–20 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

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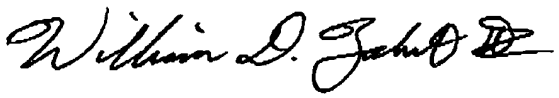
Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,



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